12.3 A Compact Low-Noise Weighted Distributed Amplifier in CMOS

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The noise figure (NF) of a front-end low-noise amplifier (LNA) places a lower bound on the sensitivity of a receiver. In a conventional LNA, there is a trade-off between the intrinsic input capacitance of the input transistors and the achievable bandwidth (BW) of the amplifier. This makes it necessary to use smaller transistors at higher gate overdrive voltages to simultaneously achieve greater BW and better NF. Unfortunately, biasing the transistor in this fashion yields a power-inefficient design. Furthermore, the need for a smaller capacitance presents a challenge to electrostatic discharge (ESD) protection of the input due to its added capacitance.

One possible way to overcome this noise-bandwidth trade-off is to use distributed amplifiers (DA), where the input and output parasitic capacitances of the individual amplification stages are absorbed into a transmission line (T-line) and become part of its real impedance. In a standard DA, the output currents of equally-weighted (identical-stages) transconductance (G_m) stages propagate through the output T-line and add coherently at the load. This leads to a broadband response fundamentally limited by the cutoff frequency of the synthetic T-lines. It has been shown that it is possible to design low-noise equally-weighted DAs at reasonable power levels [1].

Allowing the transconductance (G_m) of different stages of a DA to be different provides us with an added degree of freedom in the design and optimization of a DA. A *weighted distributed amplifier* (WDA), shown in Fig. 12.3.1, can be viewed as an analog finite-impulse-response (FIR) system. Looking at the noise in such a WDA, the noise at the output is a weighted sum of noise propagating through different paths with different weights for each noise source. We can use this property to shape the profile of the output noise power spectrum by changing the G_m coefficients of different stages. With proper choice of G_m's, the NF within a given frequency range can be reduced without a major penalty on the power consumption, gain, and input matching. This noise shaping can be applied to different noise sources in the circuit. For example, the noise current contribution of the input termination resistor R_i to the output voltage noise is weighted by:

$$\frac{R_i R_o}{4}\sum_{k=1}^{5} G_{m,k} e^{-j2\pi\cdot 2(5-k)\cdot\tau f}$$

where $G_{m,k}$ is the k-th block transconductance, τ is the T-line section delay, and f is the frequency. This is a more general result that reduces to the *sinc* function response for an equally-weighted DA. For instance, it can be used for noise profile shaping, optimization, and even dynamic noise notching at a selected frequency.

A comparison of the noise contours of a conventional five-stage DA and a five-stage WDA is shown in Fig. 12.3.2, taking into account all the active and passive noise sources. In these plots, the worst-case NF across the 3-to-10.6GHz frequency band for each design is plotted vs. the gate-source voltage and total amplifier bias current for the DA and the WDA. The contours show that the WDA can provide a lower worst-case NF under the same bias conditions across most of the operation points by taking advantage of the noise-shaping property of the WDA.

A five-stage WDA to cover the 3-to-10.6GHz frequency band has been designed and optimized in a 0.13µm CMOS process based on this methodology, where each transconductance is a cascode stage with a bandwidth-enhancement inductor L_B [2] between the equally-sized common-source (M_1) and the common-gate (M_2) transistors. An optimizer is used for transistor sizing in each of the five G_m stages resulting in transistor widths tabulated in Fig. 12.3.3. The intra-stage BW-enhancement inductors, L_B's, are sized differently in each stage to obtain equal group delays. To maintain the uniformity of the input and output T-lines, the total capacitance on different nodes must be kept the same. Considering that individual transistors have been weighted for noise optimization, this creates an opportunity to use the necessary added extrinsic capacitors to implement ESD protection diodes in a distributed fashion, as shown in Fig.12.3.3. Since the T-lines act as a very low impedance path at low frequencies, these distributed ESD protections will appear as a large aggregate ESD protector at the input and the output. Also, it is possible to use the necessary extrinsic capacitors to absorb the output capacitance of a driver or a PA on the transmit side.

In classical DA design at lower frequencies, the input and output T-lines are usually synthesized using inductors. In an integrated implementation with on-chip inductors, there always exists some mutual magnetic coupling between adjacent inductors. One approach is to minimize this mutual coupling by placing inductors far from each other. However, this results in an excessive and unnecessary area overhead in the design. An alternative is to pack the inductors together as tightly as possible and to make the mutual coupling a parameter of the design. When this is done, the mutual coupling can either increase or decrease the effective inductance experienced by each stage. By choosing an alternating winding orientation for the adjacent inductors, the positive polarity is chosen so that to the first-order, equivalent T-line impedance is

$$Z_0 \approx \sqrt{\frac{L+2M}{C}}$$

where Z_o is the intrinsic impedance, L is the T-line's unit inductance, and C is the unit capacitance. This way, not only is the area reduced by close placement of inductors, but also advantage is taken of the mutual couplings to reduce the sizing of each inductor. It should be noted that in the above argument, the fact that signals in the adjacent inductors are slightly out of phase with each other is ignored. Fortunately, in this setting the phase lead of the mutual coupling to the left compensates the phase lag of the coupling to the right to the first order.

The WDA is implemented in 0.13µm CMOS with seven metal layers. The chip is mounted on a PCB, with wirebonds for bias and digital pads and is probed at the input and output pads using RF probes. Figure 12.3.5 shows the measured S-parameters of the WDA. The WDA achieves an S_{11} of better than -12dB up to 12GHz and an S_{22} of better than -15dB up to 13GHz. The S_{21} is around +15dB from DC to 12GHz while the S_{12} is lower than -24dB across the band. The measured NF, input third-order intercept point (IIP3) and the 1dB compression point (P_{1dB}) vs. frequency are shown in Fig. 12.3.6. The NF is better than 4.5dB across the band with a minimum of 2.3dB. The WDA consumes 26mW from a 1V supply, and can be operated at different power consumption levels. For example, at 17mW of power dissipation, similar or better S_{11}, S_{22}, and S_{12} can be achieved at a slightly lower S_{21} of 11 to 13dB along with a 2.5dB minimum NF from 1 to 10.6 GHz. The WDA chip micrograph is shown in Fig. 12.3.7. It occupies 0.87×0.5mm^2 of die area including all pads. Similar or better results are achieved by this IC compared with recent broadband CMOS LNA publications [1, 3-6].

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[2] B. Analui, and A. Hajimiri, "Bandwidth Enhancement for Transimpedance Amplifier," *IEEE J. Solid-State Circuits*, pp. 1263-70, Aug. 2004.
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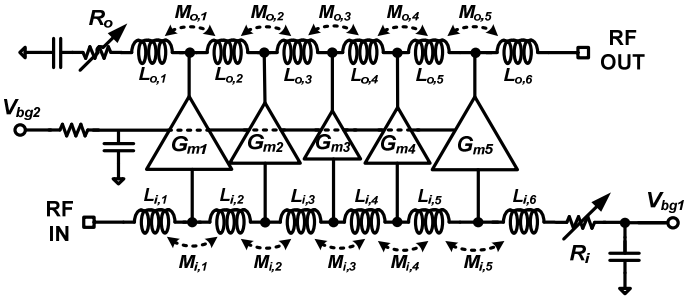


Figure 12.3.1: Architecture of the weighted distributed amplifier (WDA).

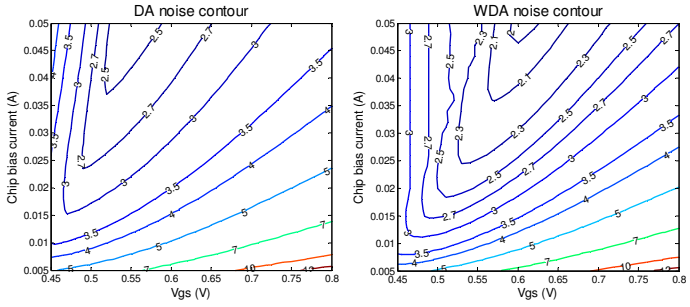
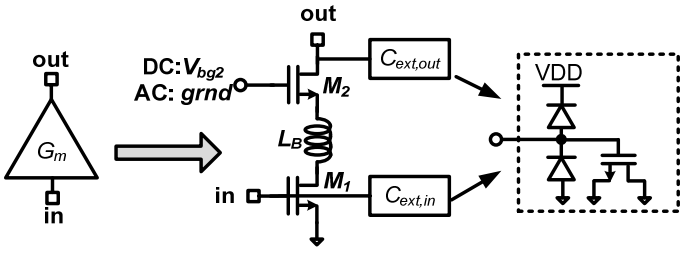


Figure 12.3.2: Noise-figure optimization contour comparison between a five-stage conventional DA and a five-stage WDA.



	G_{m1}	G_{m2}	G_{m3}	G_{m4}	G_{m5}
M_1, M_2 (um)	184/0.13	156/0.13	96/0.13	136/0.13	160/0.13
L_B (pH)	180	210	370	240	210
$C_{ext,in}$ (fF)	0	55	170	95	45
$C_{ext,out}$ (fF)	150	180	250	205	175

Figure 12.3.3: Detailed schematics of the G_m stages.

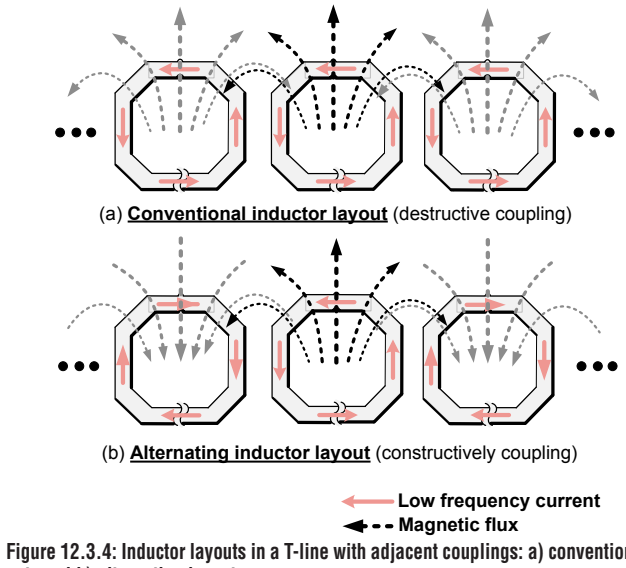


Figure 12.3.4: Inductor layouts in a T-line with adjacent couplings: a) conventional layout, and b) alternating layout.

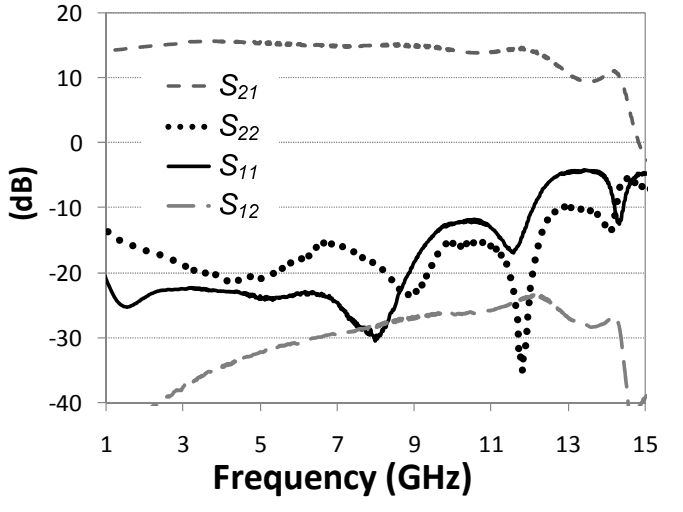


Figure 12.3.5: Measured performance: scattering parameters.

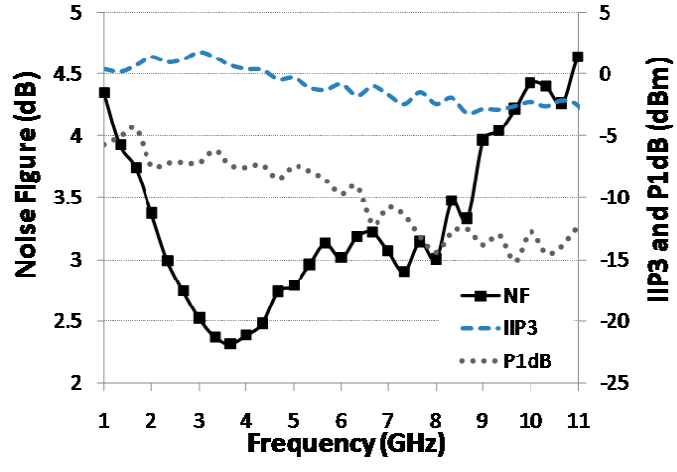


Figure 12.3.6: Measured performance: noise figure, IIP3 and P1dB.

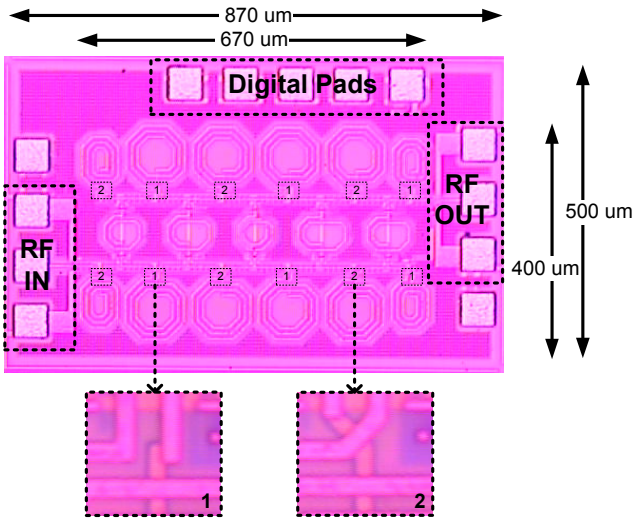


Figure 12.3.7: Chip micrograph with zoomed-in views for alternating-winding inductor layout.

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